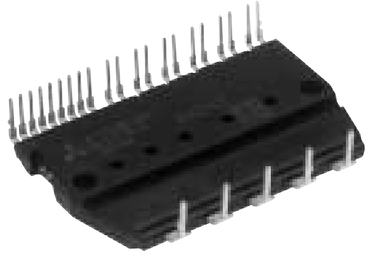
PS21563-P

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21563-P



INTEGRATED POWER FUNCTIONS

600V/10A low-loss 5th generation inverter bridge for three phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

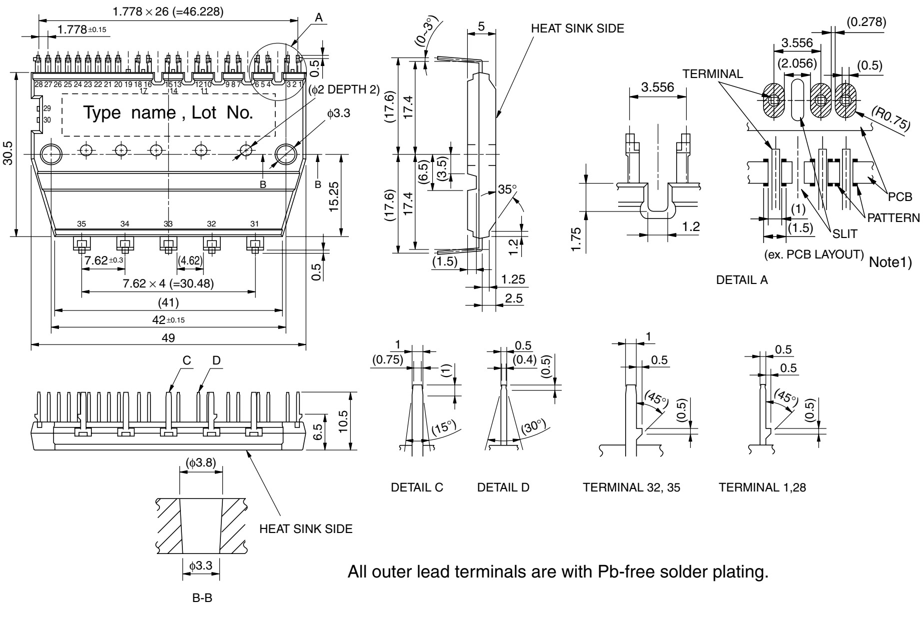
- For upper-leg IGBTS :Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTS : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3, 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



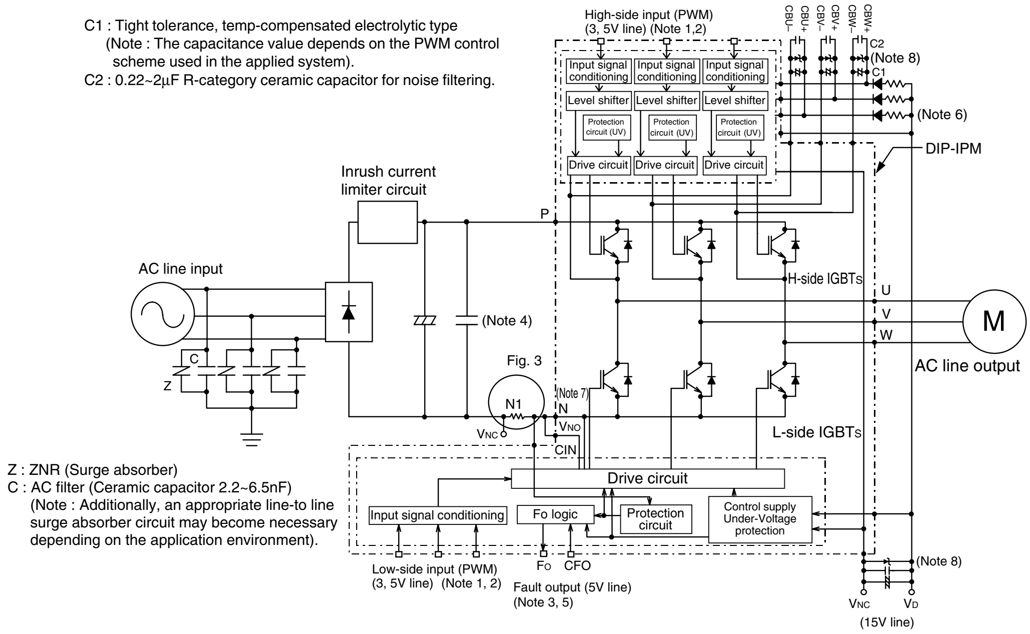
All outer lead terminals are with Pb-free solder plating.

TERMINAL CODE

1	VUFS
2	(UPG)
3	VUFB
4	VP1
5	(COM)
6	UP
7	VVFS
8	(VPG)
9	VVFB
10	VP1
11	(COM)
12	VP
13	VWFS
14	(WPG)
15	VWFB
16	VP1
17	(COM)
18	WP
19	(UNG)
20	VNO Note2)
21	UN
22	VN
23	WN
24	FO
25	CFO
26	CIN
27	VNC
28	VN1
29	(WNG)
30	(VNG)
31	P
32	U
33	V
34	W
35	N

Note 1 : In order to get enough creepage distance between the terminals, please take some countermeasure such as a slit on PCB.
2 : The 20th terminal VNO is treated as a NC in DIP-IPM ver.2, it should be connected with the terminal N outside in PS21563-P.

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

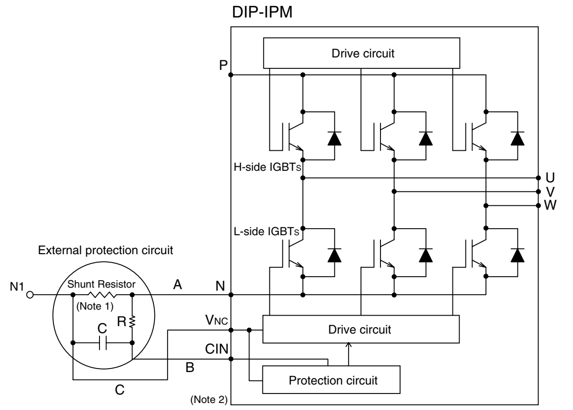


C1 : Tight tolerance, temp-compensated electrolytic type
(Note : The capacitance value depends on the PWM control scheme used in the applied system).
C2 : 0.22~2µF R-category ceramic capacitor for noise filtering.

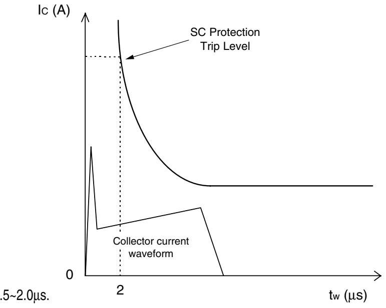
Z : ZNR (Surge absorber)
C : AC filter (Ceramic capacitor 2.2~6.5nF)
(Note : Additionally, an appropriate line-to line surge absorber circuit may become necessary depending on the application environment).

Note1: Input logic is high-active. There is a 2.5kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.
2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 8)
3: This output is open drain type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistance. (see also Fig. 8)
4: The wiring between the power DC link capacitor and the P, N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to be mounted close to these P-N1 DC power input pins.
5: Fo output pulse width should be decided by putting external capacitor between CFO and V_{NC} terminals. (Example : C_{FO}=22nF → t_{FO}=1.8ms (Typ.))
6: High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.
7: The terminal V_{NO} should be connected to the terminal N outside of DIP-IPM.
8: To prevent ICs from surge destruction, it is recommended to insert a Zener diode (24V, 1W) nearby each pair of supply terminals.

Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.



Note1: In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0µs.
2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	T_f = 25°C	10	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_f = 25°C, less than 1ms	20	A
P_C	Collector dissipation	T_f = 25°C, per 1 chip	20	W
T_j	Junction temperature	(Note 1)	–20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_f \leq 100$°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125$°C (@ $T_f \leq 100$°C).

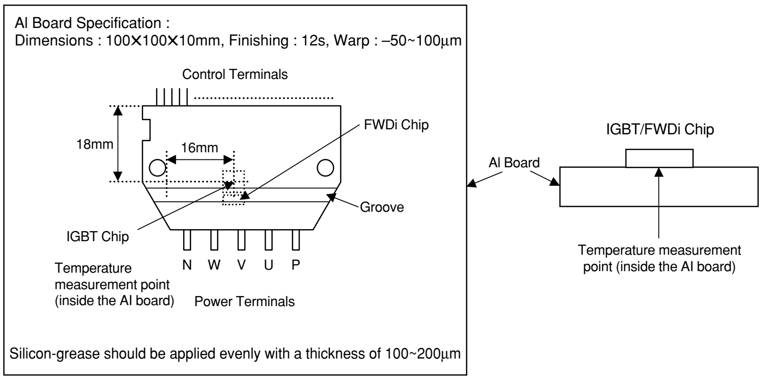
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	–0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	–0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	–0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short circuit protection capability)	V_D = 13.5~16.5V, Inverter part T_j = 125°C, non-repetitive, less than 2 µs	400	V
T_f	Module case operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, All connected pins to heat-sink plate	2500	V_{rms}

Note 2 : T_f measurement point



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	5.0	°C/W
$R_{th(j-f)F}$		Inverter FWD part (per 1/6 module)	—	—	6.5	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100µm~+200µm on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = V_{DB} = 15V V_{IN} = 5V	I_C = 10A, T_j = 25°C	—	1.60	2.10	V
			I_C = 10A, T_j = 125°C	—	1.70	2.20	
V_{EC}	FWD forward voltage	T_j = 25°C, $-I_C$ = 10A, V_{IN} = 0V		—	1.50	2.00	V
t_{on}	Switching times	V_{CC} = 300V, V_D = V_{DB} = 15V I_C = 10A, T_j = 125°C, V_{IN} = 0 ↔ 5V Inductive load (upper-lower arm)		0.60	1.20	1.80	µs
t_{rr}				—	0.30	—	µs
$t_{c(on)}$				—	0.40	0.60	µs
t_{off}				—	1.40	2.10	µs
$t_{c(off)}$				—	0.50	0.80	µs
I_{CES}	Collector-emitter cut-off current	V_{CE} = V_{CES}	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	V_D = V_{DB} = 15V V_{IN} = 5V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	5.00	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	0.40	
		V_D = V_{DB} = 15V V_{IN} = 0V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	7.00	
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	0.55	
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O circuit pull-up to 5V with 10kΩ		4.9	—	—	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		—	—	0.95	V
$V_{SC(ref)}$	Short circuit trip level	T_f = −20~100°C, V_D = 15V (Note 4)		0.45	—	0.52	V
I_{IN}	Input current	V_{IN} = 5V		1.0	1.5	2.0	mA
UV_{DBt}	Control supply under-voltage protection	T_j ≤ 125°C	Trip level	10.0	—	12.0	V
UV_{DBr}			Reset level	10.5	—	12.5	V
UV_{Dt}			Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V
t_{FO}	Fault output pulse width	C_{FO} = 22nF (Note 5)		1.0	1.8	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}		2.1	2.3	2.6	V
$V_{th(off)}$	OFF threshold voltage			0.8	1.4	2.1	V

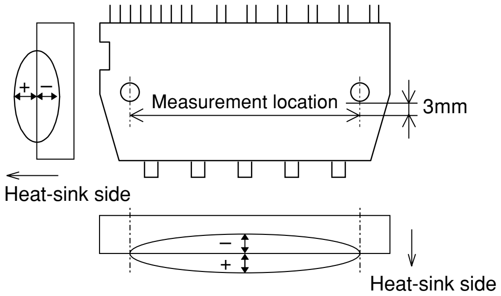
Note 4: Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

5: Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure. The fault output pulse width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO}$ [F].

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	Recommended : 0.78 N·m	0.59	—	0.98	N·m
Weight			—	20	—	g
Heat-sink flatness		(Note 6)	–50	—	100	µm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Recommended value			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-N		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			–1	—	1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal, $T_f \leq 100°C$		1.5	—	—	µs
f_{PWM}	PWM input frequency	$T_f \leq 100°C$, $T_j \leq 125°C$		—	—	20	kHz
I_O	Allowable r.m.s. current	$V_{CC} = 300V$, $V_D = V_{DB} = 15V$, P.F = 0.8, sinusoidal output $T_f \leq 100°C$, $T_j \leq 125°C$ (Note 7)	f_{PWM} = 5kHz	—	—	6.5	Arms
			f_{PWM} = 15kHz	—	—	4.0	
PWIN(on)	Allowable minimum input pulse width	(Note 8)		0.3	—	—	µs
PWIN(off)		$200 \leq V_{CC} \leq 350V$, $13.5 \leq V_D \leq 16.5V$, $13.0 \leq V_{DB} \leq 18.5V$, $-20°C \leq T_f \leq 100°C$, N-line wiring inductance less than 10nH (Note 9)	Below rated current	0.5	—	—	
			Between rated current and 1.7 times of rated current	0.5	—	—	
			Between 1.7 times and 2.0 times of rated current	0.7	—	—	
V_{NC}	V_{NC} variation	Between V_{NC}-N (including surge)		–5.0	—	5.0	V

Note 7 : The allowable r.m.s. current value depends on the actual application conditions.
8 : The input pulse width less than PWIN(on) might make no response.
9 : IPM might not work properly or make response for the input signal with OFF pulse width less than PWIN(off). Please refer to Fig.7.

Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

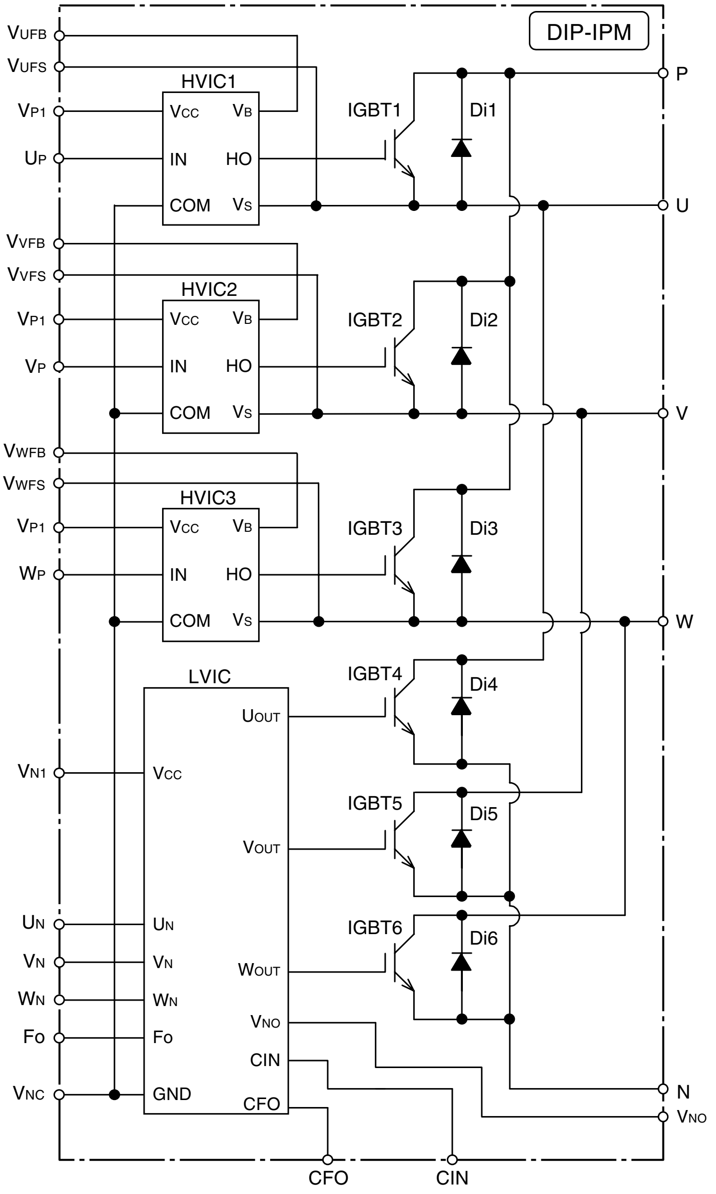
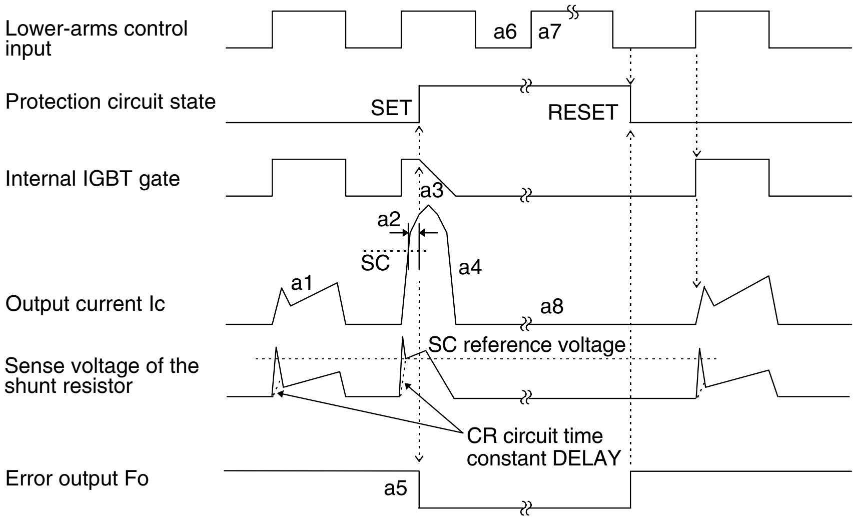


Fig. 5 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

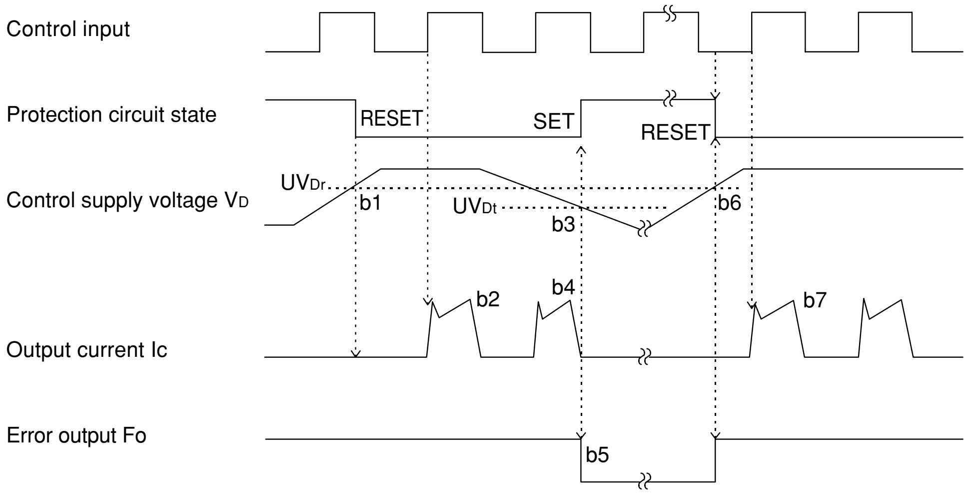
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. F_O timer operation starts : The pulse width of the F_O signal is set by the external capacitor C_{FO}.
a6. Input “L” : IGBT OFF.
a7. Input “H” : IGBT ON.
a8. IGBT OFF in spite of input “H”.



[B] Under-Voltage Protection (Lower-arm, UV_D)

b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UV_{Dt}).
b4. IGBT OFF in spite of control input condition.
b5. F_O operation starts.
b6. Under voltage reset (UV_{Dr}).
b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-arm, UV_{DB})

c1. Control supply voltage rises : After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip (UV_{DBt}).
c4. IGBT OFF in spite of control input condition, but there is no F_O signal output.
c5. Under voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.

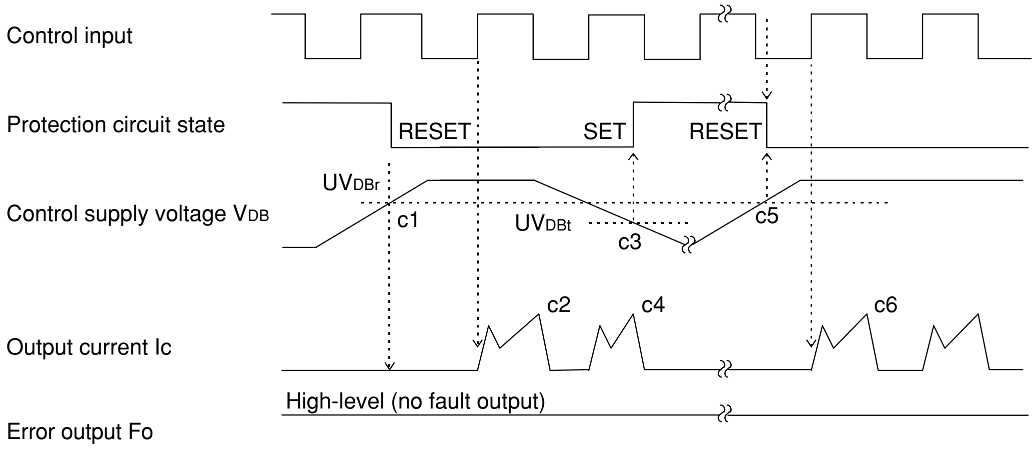
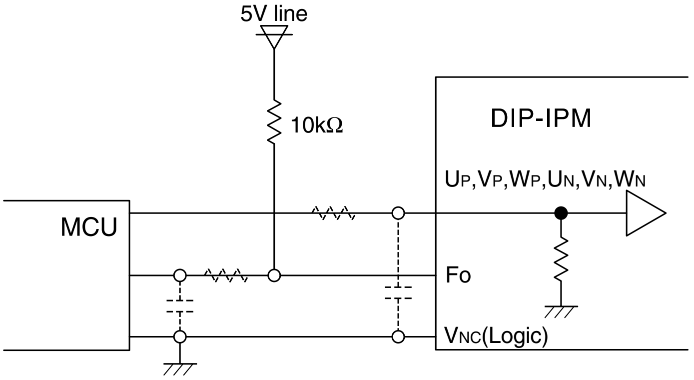
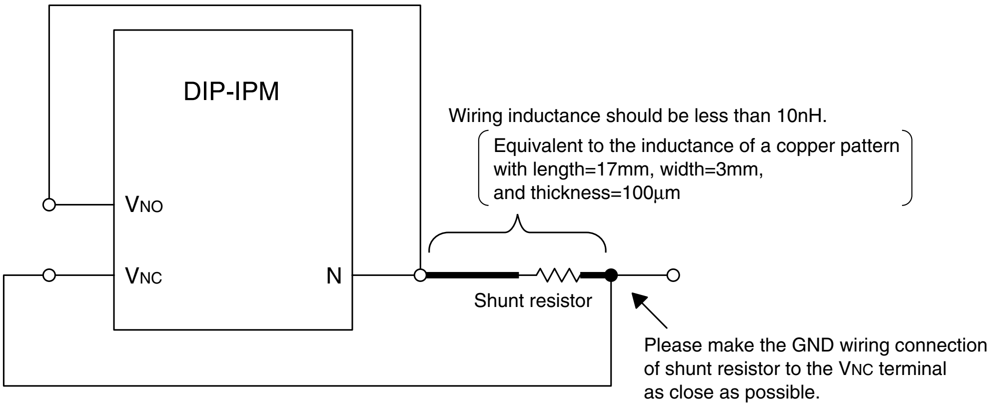


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
The DIP-IPM input section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 7 WIRING CONNECTION OF SHUNT RESISTOR

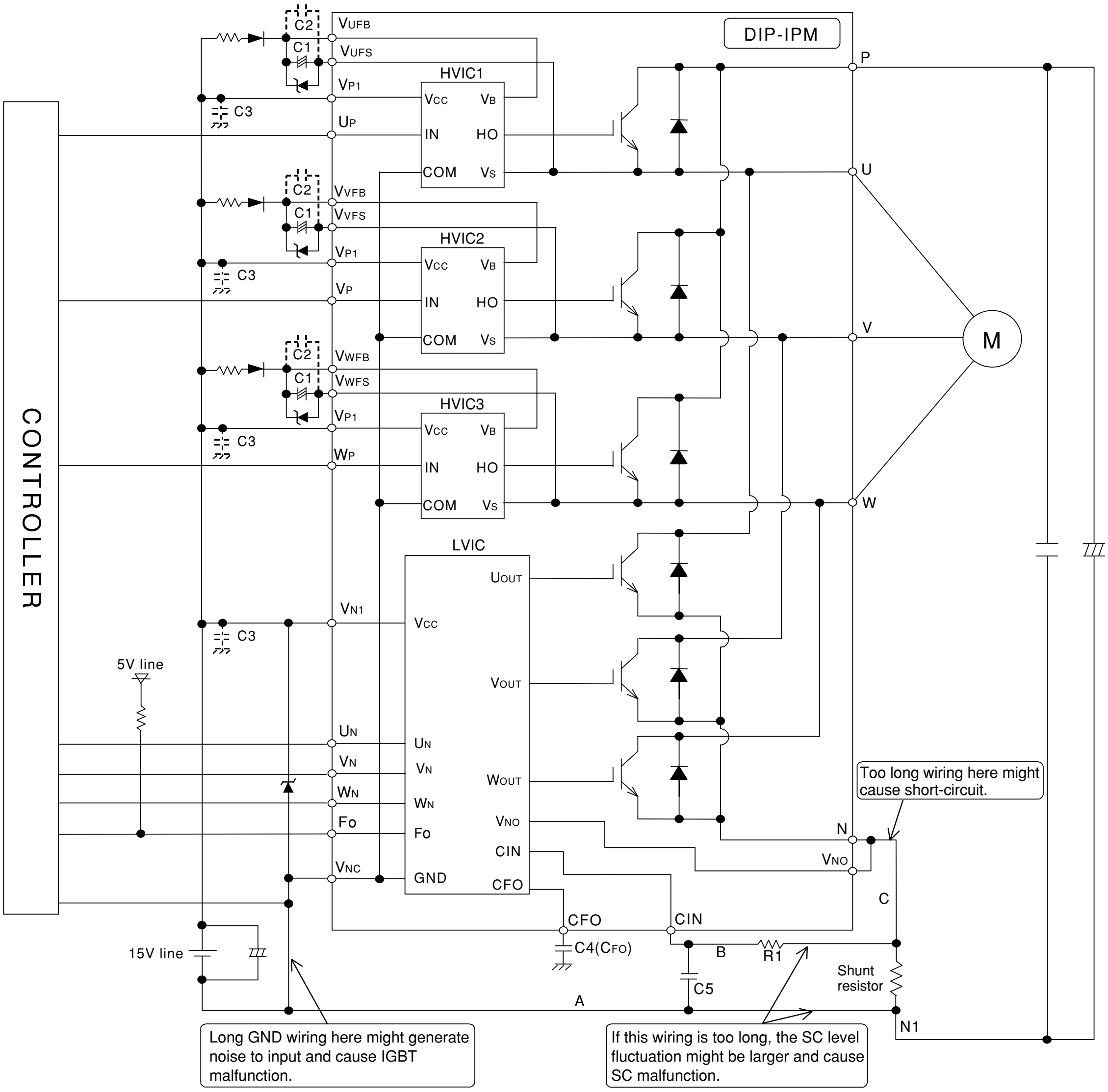


Wiring inductance should be less than 10nH.
(Equivalent to the inductance of a copper pattern with length=17mm, width=3mm, and thickness=100μm)

Please make the GND wiring connection of shunt resistor to the V_{NC} terminal as close as possible.

Fig. 8 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE

C1:Tight tolerance temp-compensated electrolytic type
C2,C3: 0.22~2µF R-category ceramic capacitor for noise filtering.



Too long wiring here might cause short-circuit.

Long GND wiring here might generate noise to input and cause IGBT malfunction.

If this wiring is too long, the SC level fluctuation might be larger and cause SC malfunction.

Note 1 : To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)
2 : By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
3 : FO output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.
4 : FO output pulse width is determined by the external capacitor between CFO and VNC terminals (CFO). (Example : CFO = 22 nF → tFO = 1.8 ms (typ.))
5 : The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.
6 : To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.
7 : Please set the C5R1 time constant in the range 1.5~2µs.
8 : Each capacitor should be located as nearby the pins of the DIP-IPM as possible.
9 : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 pins should be as short as possible. Approximately a 0.1~0.22µF snubber capacitor between the P-N1 pins is recommended.
10 : The terminal VNO should be connected with the terminal N outside.
11 : To prevent ICs from surge destruction, it is recommended to insert a Zener diode (24V, 1W) nearby each pair of supply terminals.